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CENTRAL FAX CENTER****JUN 15 2007**Remarks:

Reconsideration of the application, as amended herein, is respectfully requested.

Claims 1 - 8 are presently pending in the application. Claims 1, 5 and 6 have been amended.

In item 4 of the above-identified Office Action, claims 1 - 6 and 8 were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over U. S. Patent No. 6,981,179 to Shigemasa et al ("SHIGEMASA") in view of U. S. Patent No. 6,990,607 to Sim et al ("SIM"). In item 5 of the Office Action, claim 7 was rejected under 35 U.S.C. § 103(a) as allegedly being obvious over SHIGEMASA in view of SIM, and further in view of U. S. Patent Application Publication No. 2002/0066056 to Suzuki et al ("SUZUKI").

Applicants respectfully traverse the above rejections, as applied to the amended claims.

More particularly, Applicants' invention is directed to an integrated module which allows the carrying out of a self-test of an integrated memory wherein no additional BIST hardware has to be provided for this purpose. As discussed in connection with Fig. 1 of the instant application, the integrated module 1 comprises a memory 2, for storing code or

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data, and a microcontroller 3, which is connected to both an external terminal P of the module 1 and to the memory 2. Data transfers via the external terminal P of the module are controlled by the microcontroller 3. As discussed in connection with Fig. 2 of the instant application, the microcontroller 3 includes, among other things, a central processing unit (CPU) 4 and an internal memory, which can be utilized as a command memory 5 and as a defect data memory 6.

Claim 1 of the instant application has been amended to recite, among other limitations:

a defect data memory for storing addresses of the memory cells of said memory which have been detected as defective, said addresses being generated during the functional testing, said addresses being stored in said defect data memory under control of said microcontroller, said addresses further being read out under control of said microcontroller, to outside of the integrated module. [emphasis added by Applicants]

Similarly, Applicants' independent claim 5 has been amended to recite, among other limitations:

storing addresses of memory cells of the memory which have been detected as defective during the functional testing in a defect data memory, said addresses being stored in said defect data memory under control of said microcontroller; and

reading-out the addresses of the memory cells of the memory which have been detected as defective during functional testing stored in the defect data memory, under the control of the microcontroller, to outside the integrated module for further evaluation.
[emphasis added by Applicants]

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As such, Applicants' claimed invention requires, among other things, both: 1) the storing of addresses, under control of the microcontroller, of memory cells of the memory which have been detected as defective during the functional testing; and 2) the reading-out of the stored addresses, under the control of the microcontroller, of the memory cells of the memory which have been detected as defective, to outside the integrated module. The amendments to claims 1 and 5 are supported by the specification of the instant application, for example, by originally filed claim 6, as well as, page 10 of the instant application, lines 13 - 26, which state:

Before the beginning of the test operation, a command sequence for carrying out a test sequence that is executed on the microcontroller is read in from the test system 7. This process is controlled by the CPU 4, the command sequence being loaded into the command memory 5 (step A). In step B, the test is executed by the CPU 4 from a start address of the internal memory. Accordingly, test data are written to the memory 2 by the CPU 4. In step C, the data are read out again from the memory 2 under the control of the CPU 4 and corresponding defect data are stored in the defect data memory 6 under the control of the CPU 4. Afterward, the defect data stored in the defect data memory 6 are read out to outside the module 1, under the control of the CPU 4, to the test system 7 in order to evaluate the functional testing (step D). [emphasis added by Applicants]

The SHIGEMASA and SIM references, cited in the Office Action, fail to teach or suggest an integrated module including all limitations of Applicants' amended claims. For example, the

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SHIGEMASA reference fails to teach or suggest, among other limitations of Applicants' claims, either of, the storing of addresses, under control of the microcontroller, of memory cells of the memory which have been detected as defective during the functional testing, or the reading-out of the stored defective memory addresses, under the control of the microcontroller. In fact, page 3 of the Office Action states, in part:

Shigemasa et al. does not explicitly teach the module comprising of a defect data memory for storing addresses of the memory cells of said memory which have been detected as defective, said addresses being generated during the functional testing, said addresses being stored in said defect data memory under control of said microcontroller. [emphasis added by Applicants]

Rather, pages 3 - 4 of the Office Action go on to cite the **SIM** reference, in combination with **SHIGEMASA**, as allegedly teaching the storing of the addresses of memory cells detected as being defective during functional testing, under control of the microcontroller. However, Applicants' respectfully disagree that the **SIM** reference would supply a teaching or suggestion, in combination with the **SHIGEMASA** reference, of all of the elements of Applicants' amended claims.

More particularly, the **SIM** reference discloses a system and method for adaptive storage and caching of a defect table in a mass storage device. In a mass storage device, a defect table

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is stored on a recording medium. During production of the mass storage device, the mass storage device is tested to determine which portions, if any, of the recording medium are not sufficiently reliable for writing and reading of data. In **SIM**, the addresses of each of the unreliable portions are stored on the recording medium in the defect table. See, for example, col. 1 of **SIM**, lines 13 - 16.

However, according to **SIM**, during operation of conventional mass storage devices, the defect table on the recording medium is read and the entire defect table on the recording medium is cached in a defect table in memory on the microcontroller or microprocessor of the mass storage device. See, col. 1 of **SIM**, lines 38 - 42. Additionally, **SIM** discloses that, when the microcontroller or microprocessor receives a write command, the microcontroller or microprocessor will determine that the addresses indicated in the cached defect table that will not be used for writing data. See, col. 1 of **SIM**, lines 48 - 51. Thus, in **SIM**, the defect table on the recording medium is referred to by the microcontroller or microprocessor to determine which portions of the recording medium are not to be used. This teaching of **SIM** makes clear that the addresses stored in the cached defect table of **SIM** are only used for internal processing by the microcontroller or microprocessor. In contrast to the teachings of **SIM**, Applicants' instant

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claims require, among other things, that defect data stored in the defect data memory be read out to outside the module under the control of the microcontroller. This facilitates one of the goals of the instant invention, i.e., to have the read-out data evaluated by an external test system connected to an external terminal P. See, for example, Fig. 2 of the instant application.

As such, neither SHIGEMASA, nor SIM, teach or suggest, among other limitations of Applicants' claims, the reading-out of addresses of the memory cells of the memory which have been detected as defective during functional testing , under the control of the microcontroller, to outside the integrated module. As such, Applicants' claims are believed to be patentable over the SHIGEMASA and SIM references, whether taken alone, or in combination.

Additionally, the SUZUKI reference, cited in the Office Action in combination with SHIGEMASA and SIM against Applicants' dependent claim 7, does not cure the above-discussed deficiencies of the SHIGEMASA and SIM references. As such, Applicants' amended claims are believed to be patentable over SHIGEMASA, SIM and SUZUKI, whether taken alone, or in combination.

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It is accordingly believed that none of the references, whether taken alone or in any combination, teach or suggest the features of claims 1 and 5. Claims 1 and 5 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claims 1 or 5.

In view of the foregoing, reconsideration and allowance of claims 1 - 8 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemmer LLP, No. 12-1099.

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Respectfully submitted,



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